An Efficient Heuristic Approach for Irregular LDPC Code Construction with Low Error

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Abstract—Low-Density Parity-Check (LDPC) codes are increasingly being considered as good candidates for the next-generation FEC codes in high throughput wireless and recording applications. Trapping sets (TSs) are known to cause error floors in regular and irregular low-density parity-check (LDPC) codes. In existing algorithm, namely the Progressive-Edge-Growth Approximate-minimum-Cycle-Set-Extrinsic-message-degree (PEG-ACSE) method that aims to avoid small elementary trapping sets (ETSs), particularly detrimental ETSs during the code construction process which lowers error floor effectively. But as the length of code increases computational complexity and Error Floor increases using this conventional method. We proposed an efficient heuristic approach which reduces error floor and computational complexity in an irregular LDPC code design process. In our proposed method parity check matrices are generated randomly and mutation operation is performed on this matrix. Corresponding Tanner graph is plotted for each matrix. Messages are transmitted over Additive White Gaussian Noise (AWGN) channel, Bit Error Rate (BER), Frame Error Rate (FER) and computational complexity is calculated through our proposed algorithm. Results from simulations show that the codes constructed using the proposed method produce lower error rates with reduced computational complexity, particularly at the high signal-to-noise (SNR) region, compared with codes constructed using other PEG-ACSE based algorithms.

Index Terms—Irregular LDPC codes, heuristic approach, parity check matrix, trapping set, mutation operation.

I-INTRODUCTION

A category of codes possessing features and performance identical to that of turbo codes has been rediscovered following the unparalleled success of the latter. Codes of this category are termed as low-density parity-check (LDPC) codes [1] [14]. One of the capacity approaching error correction code that has emerged as an efficient competitor over several vital channels is the Low-density parity-check (LDPC) code. They are appropriate for use in extremely efficient parallel decoding algorithms and have displayed good performance. Photographs also known as base graphs or projected graphs are used as the basis for a well-known construction of LDPC codes [2]. Efficient encoding of LDPC codes that have a block length up to some thousand bits may be difficult if the codes do not have any algebraic structure [4].

A category of linear codes called Low-density parity-check (LDPC) codes have very few number of 1’s in parity check matrix. LDPC codes may be represented by a degree sequence, which signifies the probability of discovering a specified number of ones in either the rows or the columns of the parity check matrix. If a fixed number of ones is present in each rows and each columns then the LDPC code is said to be regular, otherwise, it is said to be irregular [3] [15]. LDPC codes can be decoded using several individually derived methods [12], such as, Believe Propagation (BP), Sum-Product (SP), and Message Passing (MP) [12] [16]. Very low error rate is necessary for several coding applications like satellite communications, Ethernet transmission, and data storage applications. Therefore, construction of practical tools for anticipating error floors and assessing the success of LDPC codes in the low frame error rate region is a significant problem [6].

In the presence of additive white Gaussian noise, detecting the major error events that contribute to the majority of the error probability at high SNR is the most difficult task of calculating the error ‘floor’ of a code (and decoder) (AWGN) [10] [17]. A better performance than regular LDPC codes is achieved by irregular LDPC codes at low SNR values [5]. Two stages exist in the construction of irregular codes. The first stage selects a profile that represents the required number of columns and rows of each weight. The second stage constructs the parity-check matrix that realizes the specified profile [7]. The parity-check matrix of a code can be regarded as describing a bipartite graph with “variable” vertices representing the columns and “check” vertices representing the rows. An edge connecting a variable to a check is represented by each non-
zero entry of the matrix [8]. Codes that contain 4 cycles are usually rejected by the pseudo-random process that constructs the irregular codes [9]. Design of irregular codes described on graphs and computation of the convergence threshold of a specified collection of codes for diverse decoding algorithms have been given much importance [11]. In addition to providing flexibility and low encoding/decoding complexity, the irregular LDPC codes have competitive performance [13] [18].

II-Related work

Olgica Milenkovic et al. [19] have calculated the asymptotic, normalized distributions of a category of combinatorial configurations in random, regular, binary low-density parity-check (LDPC) code ensembles. Trapping and stopping sets have been among the considered configurations. A crucial role is played by the subsets of variable nodes in the Tanner graph of a code that is represented by these sets in calculating the height and point of onset of the error-floor in its performance curve. Large deviation theory and statistical methods based techniques have been used in the derivations for enumerating random-like matrices. Setting that comprise more broad structural entities such as sub codes and/or minimal codeword’s which are known to represent the significant properties of soft-decision decoders of linear block codes could also employ these techniques.

Jinghu Chen et al. [20] have proposed a quasi-cyclic extension approach to create irregular low-density parity-check (LDPC) codes. The created LDPC codes have been subjected to comparatively less undetected errors and have demonstrated a relatively low error floor in the high signal-to-noise ratio (SNR) region when decoded iteratively. LDPC codes have remained efficiently encodable if developed based on the proposed scheme.

Sang Hyun Lee et al. [21] have proposed a trellis based simple design technique for creating good low-density parity-check (LDPC) codes with comparatively decreased code rates. They have enhanced the distribution of cycles created by the columns present in the parity-check part of the parity-check matrix by employing a trellis search method for design of a pre-assigned sub matrix for a simple encoding in the parity-check matrix. In addition, several practical applications at that time have preferred a class of structured LDPC codes and accordingly the proposed algorithm has been extended. The codes constructed by traditionally used greedy design algorithms have been proved to be outperformed, by means of simulation results.

Benjamin Smith et al. [22] have proposed a numerical method for decreasing the decoding complexity of long-block-length irregular low-density parity-check (LDPC) codes. In binary-input memory less symmetric channels and iterative message-passing decoding algorithms with a parallel update schedule, this design methodology could be employed. The number of operations necessary to perform a single decoding iteration and the number of iterations necessary for convergence that have been incorporated in a new complexity measure has been considered as a significant feature of the proposed optimization method. They have demonstrated that density-evolution and extrinsic information transfer chart analysis of the code could be used to precisely assess the complexity measure. They also presented a sufficient condition for the convexity of the complexity measure in the variable edge-degree distribution. In case it is not satisfied the numerical experiments have indicated that still a unique local minimum exists. The results presented in the article demonstrated that when the decoding complexity is constrained, the threshold-optimized codes have been substantially outperformed by the complexity-optimized codes at long block lengths within the ensemble of irregular codes.

Xia Zheng et al. [23] have introduced a parameter ‘e’ to determine an elementary trapping set induced number of “distinguishable” cycles in the connected sub graph. In addition, code generating algorithm that aims to prevent small elementary trapping sets (ETSs), specifically detrimental ETSs called Progressive-Edge-Growth Approximate-minimum-Cycle-Set-Extrinsic-message-degree (PEG-ACSE) method has been proposed. Theorems that calculate the least possible ETSs produced by PEG construction algorithms in general have also been developed. The features of the codes constructed using the proposed method has been compared with those constructed using PEG only or PEG-Approximate-minimum-Cycle-Extrinsic-message-degree (PEG-ACE) techniques. Simulation results have demonstrated that lower error rates compared to codes constructed using other PEG-based algorithms especially at the high signal-to-noise (SNR) region has been produced by the codes constructed using the proposed PEG-ACSE method.

In this paper, we propose an effective irregular LDPC code design to reduce the computational complexity and error floors. The paper is organized as - Section III describes the construction of irregular LDPC codes by using heuristic approach, Section IV deals with simulation results and section V concludes the paper.

III-R CONSTRUCTION OF IRREGULAR LDPC CODES
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The primary objective of the proposed heuristics technique is mainly reduction in computational complexity and error floor in designing of LDPC codes. The proposed algorithm in this paper addresses this problem up to maximum extend. The irregular LDPC codes are constructed by randomly generating a parity check matrix of ‘m’ rows and ‘n’ columns. Tanner graph is plotted for this randomly generated parity check matrix which mainly contains variable nodes and check nodes.

Let, The sample parity check matrix ‘H’ with 20 columns and 10 rows are represented as follows :

![Sample Parity Check Matrix](image)

**Fig 1:** Tanner Graph for parity check matrix (20, 10) of proposed algorithm

**Variable-node**
Correspond to bits of the codeword or equivalently, to columns of the parity check matrix. Hence, there are ‘n’ v-nodes in the Tanner Graph of parity check matrix.

**Check-nodes**
Correspond to parity check equations or equivalently, to rows of the parity check matrix. There are ‘m’ check-nodes in the Tanner Graph of parity check matrix.

**Mutation**
It is modification of a given matrix to find a better solution. The matrix is modified by randomly changing the positions zeros and ones in rows and columns of matrix generated randomly using our proposed algorithm, which may give better performance.

In tanner graph shown in Fig. 1, the upper v-nodes are called variable nodes or message nodes and the bottom c-nodes are called parity nodes or check nodes. The messages are exchanged between v-nodes and c-nodes with the edges of the graph which act as the information pathways. The tanner graph is also called as bipartite graph. The term ‘bipartite’ means that same type of nodes should not be connected, i.e. the c-node should not be connected to another c-node. In a graph the jth check node is connected to the ith variable node and if, the (i, j)th elements of the parity check matrix is one, i.e. ‘\( h_{ij} = 1 \),

**Algorithm**
Step 1: Generate parity check matrix for irregular LDPC code randomly.
Step 2: Perform mutation operation on this matrix generated randomly.
Step 3: Evaluate each matrix over AWGNC for performance.
Step 4: Best performing matrix is final designed matrix for constructed LDPC codes.
Step 5: Performance is evaluated by considering BER, FER and computational complexity.
Step 6: Implement the conventional method PEG-ACSE algorithm
Step 7: Compare the result of our proposed algorithm with matrix constructed using PEG-ACSE algorithm.

**Discussion**

All zero codeword's with BPSK type modulation is transmitted through Additive white Gaussian Noise channel (AWGNC). Codeword are decoded using belief propagation (BPA) algorithm. Bit Error Rate (BER), Frame Error Rate (FER) and computational complexity is calculated. MATLAB Platform is used for results and compared with conventional method PEG-ACSE method.

**IV- Simulation Results**

The performance of the proposed heuristic method for irregular LDPC code design is implemented and evaluated on MATLAB platform. Simulation results confirmed that the proposed approach performs efficiently with low computation complexity, Bit error rate (BER) and Frame error rate (FER). Proposed heuristic approach is also compared with PEG-ACSE approach for different code lengths.

<table>
<thead>
<tr>
<th>Code Length</th>
<th>Proposed Alg. BER</th>
<th>PEG-ACSE BER</th>
<th>Proposed Alg. FER</th>
<th>PEG-ACSE FER</th>
<th>Proposed Alg. CPU time in sec</th>
<th>PEG-ACSE CPU time in sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>(20,10)</td>
<td>0.050</td>
<td>0.089</td>
<td>0.326</td>
<td>0.602</td>
<td>0.256</td>
<td>0.969</td>
</tr>
<tr>
<td>(40,20)</td>
<td>0.081</td>
<td>0.100</td>
<td>0.579</td>
<td>0.897</td>
<td>0.893</td>
<td>7.183</td>
</tr>
</tbody>
</table>

Fig 2: Comparison of Bit Error Rate, Frame Error rate for (60, 30) Matrix
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| (60,30) | 0.096 | 0.098 | 0.767 | 0.921 | 2.028 | 22.527 |
| (80,40) | 0.101 | 0.102 | 0.868 | 0.941 | 4.451 | 58.071 |
| (100,50) | 0.102 | 0.105 | 0.918 | 0.987 | 7.575 | 111.07 |
| (120,60) | 0.105 | 0.106 | 0.970 | 1 | 12.581 | 188.58 |

V- Conclusion

In this paper irregular low density parity check codes based on the heuristic approach are designed. The computational complexity in the designed irregular LDPC codes is reduced by performing mutation operation on the randomly generated parity check matrices. Results when compared to the other existing conventional PEG-ACSE algorithm, it is clear that proposed method provides smaller bit and frame error rates. Moreover, the heuristic approach offers low computational complexity and meets the near Shannon limit.

REFERENCES


